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U.S. UTILITY Patent Application

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APPL NUM 10061517	FILING DATE 01/31/2002	CLASS <del>324</del> 714	SUBCLASS 704	GAU <del>2853</del>	EXAMINER <i>Heady</i>
<b>**APPLICANTS:</b> Harres Daniel; 2133 <i>KCR VEROS</i>					
<b>**CONTINUING DATA VERIFIED:</b> <i>None 6/9/2004</i>					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> <i>None 8/9/2004</i>					
PG-PUB <input type="checkbox"/>		DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>	
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		ATTORNEY DOCKET NO 091-0124	
Verified and Acknowledged Examiners's initials		<i>je</i>			
TITLE : Built-in test signal attenuation circuit					
U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)					

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	Print Claim for O.G.
Assistant Examiner		<b>DRAWING</b>	
		Sheets Drwg.	Figs. Drwg. Print Fig.
Primary Examiner		Application Examiner	
<b>PREPARED FOR ISSUE</b>			
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>WARNING:</b> The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	

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